

*Fig. 1*

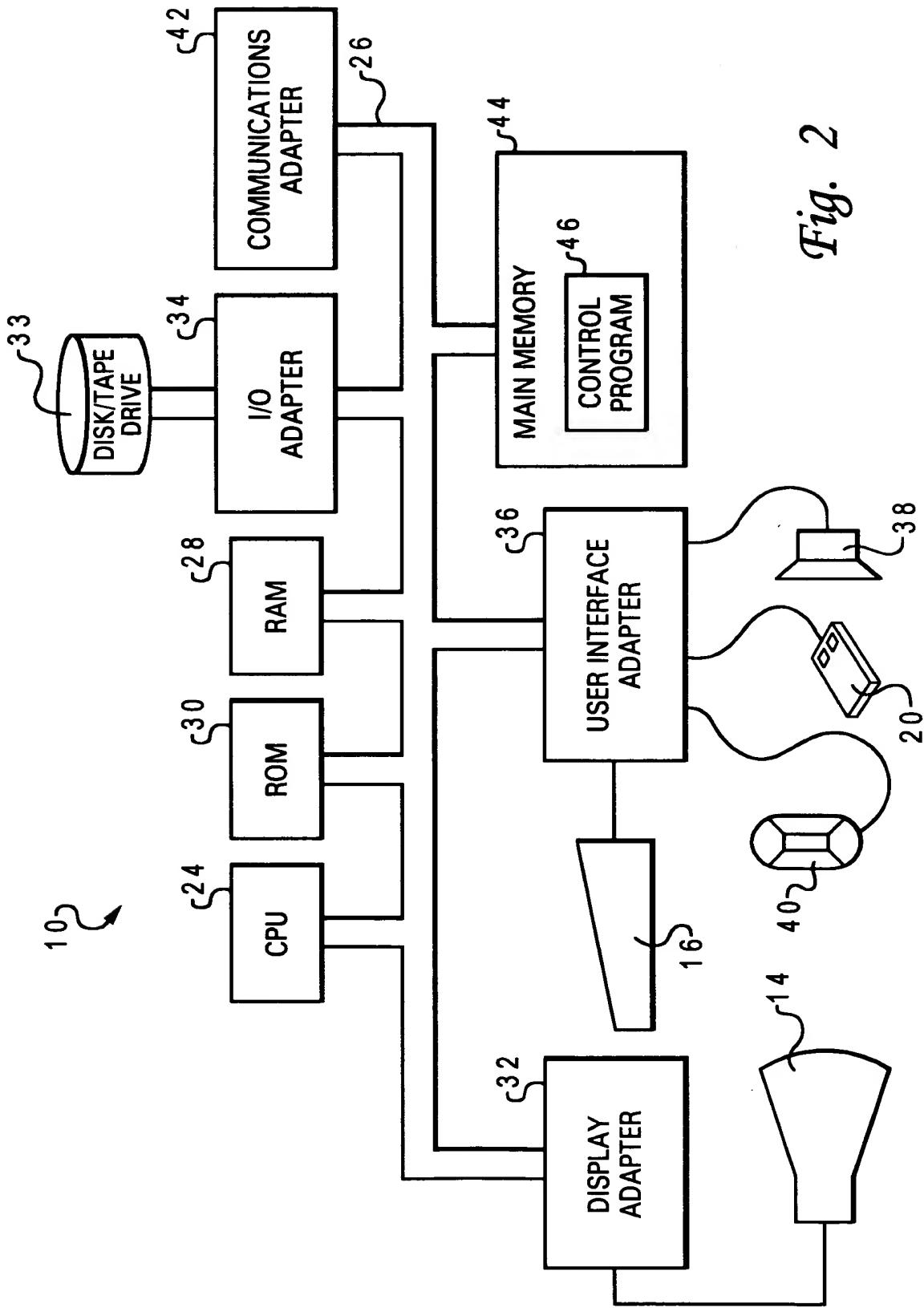
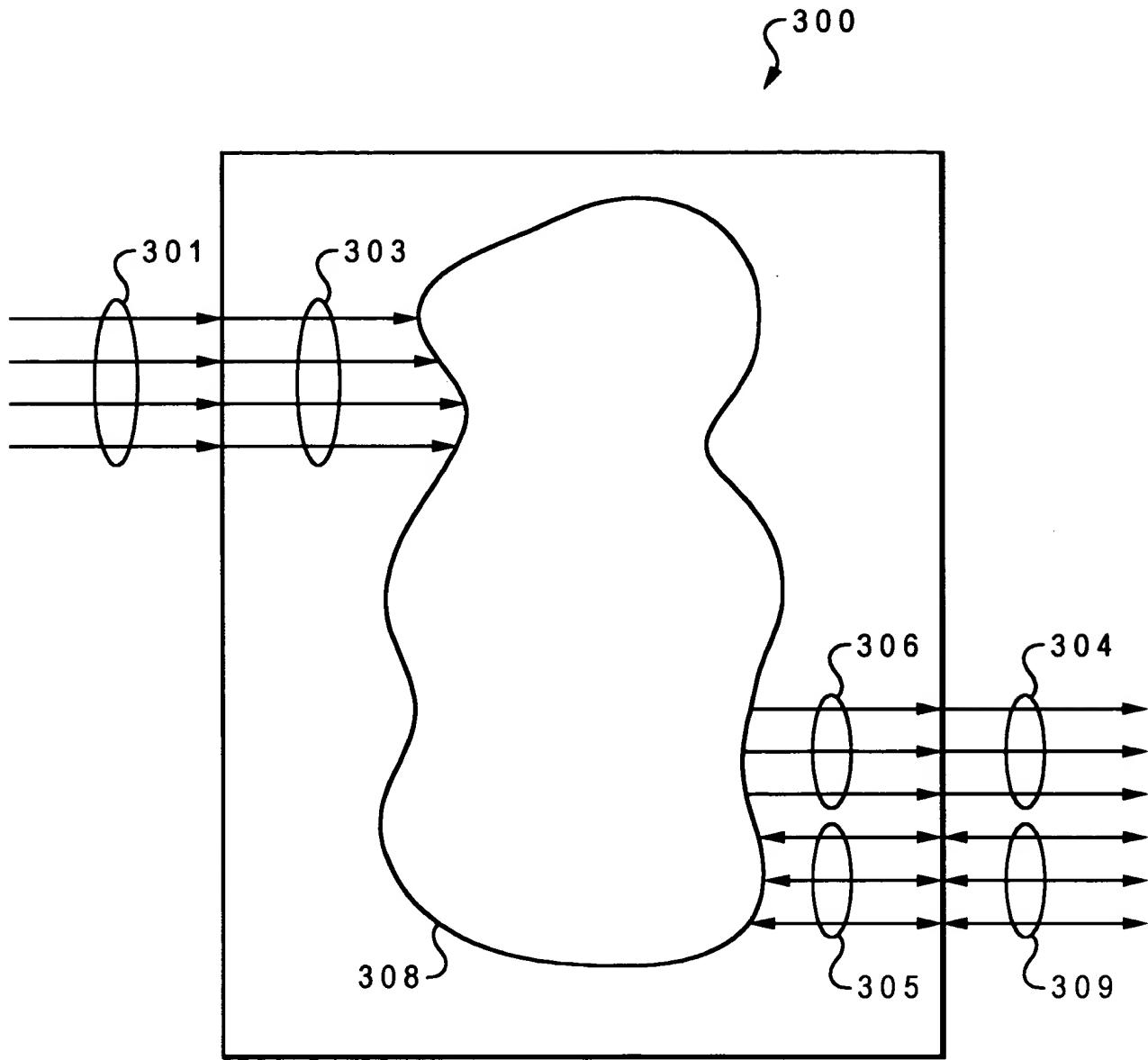


Fig. 2



*Fig. 3A*

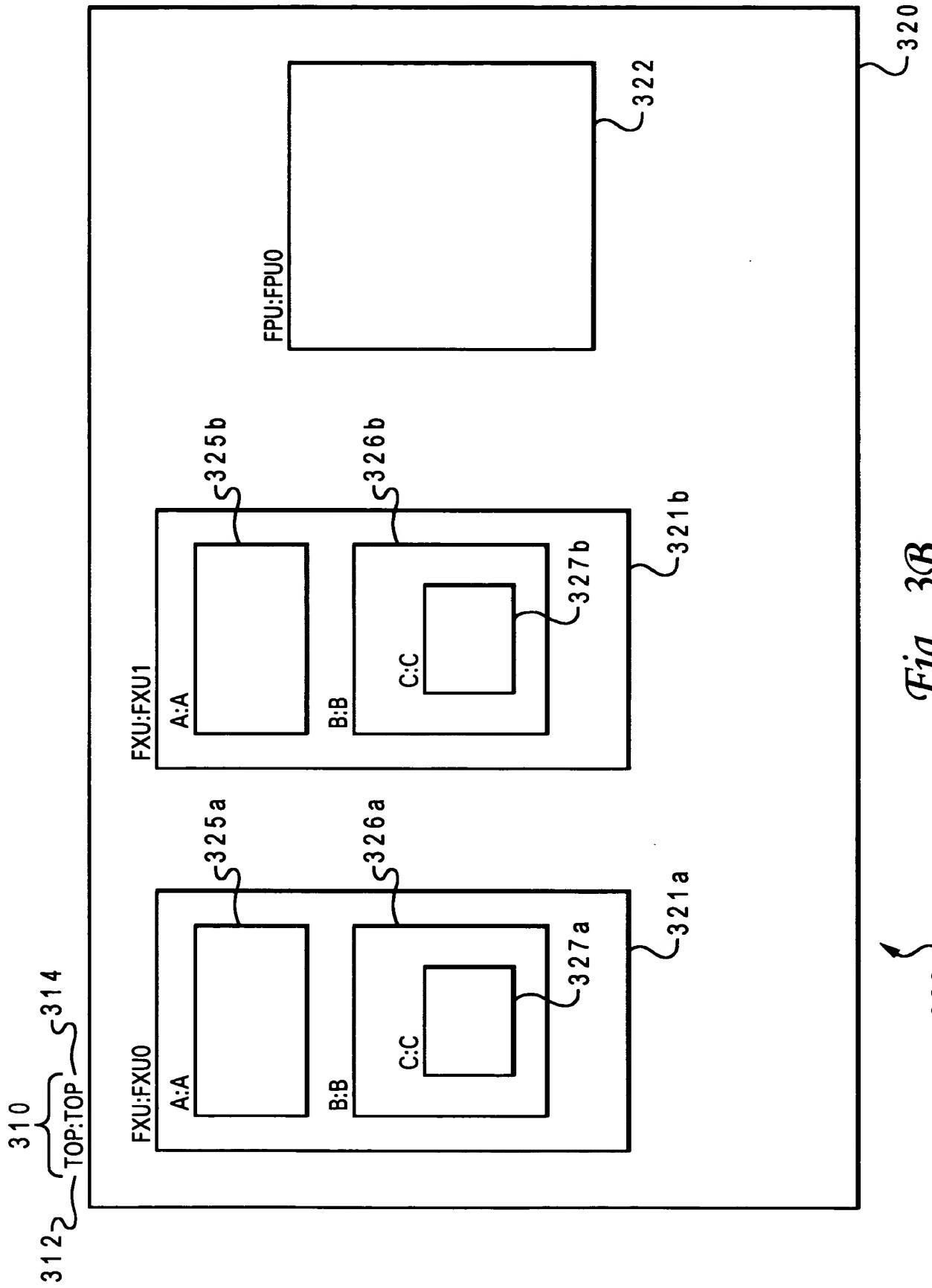


Fig. 3B

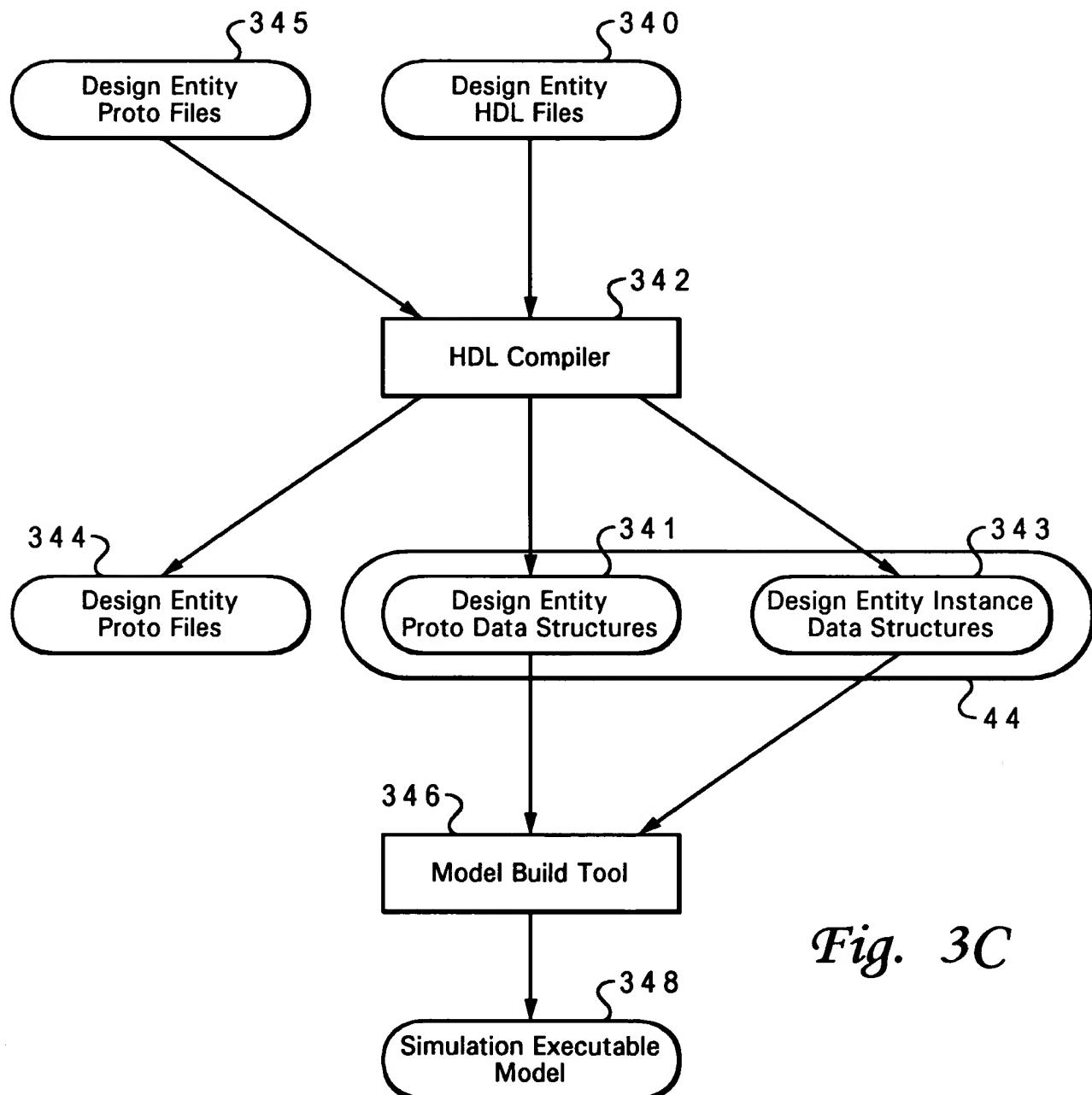


Fig. 3C

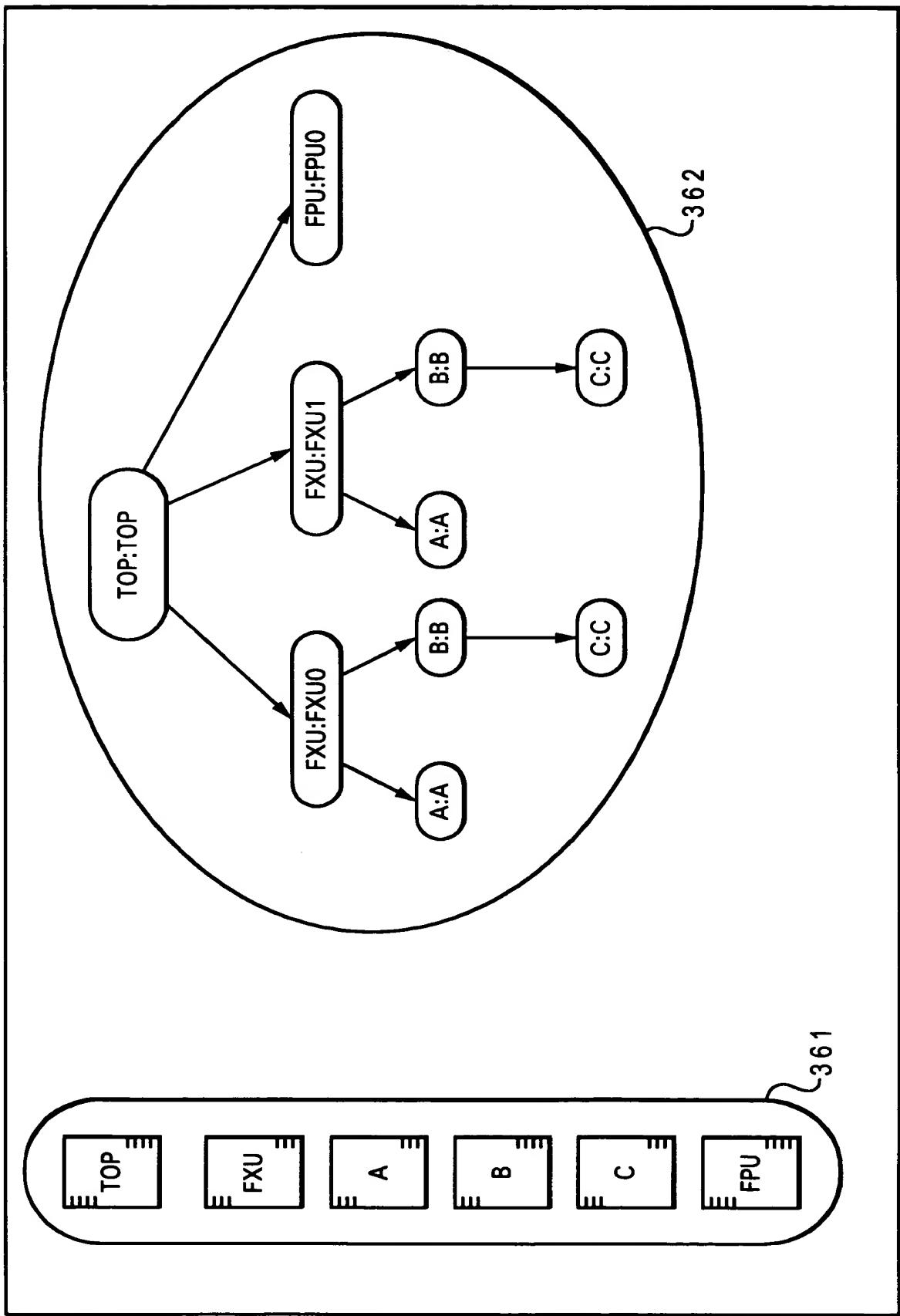


Fig. 3D

CODE: 0000000000000000

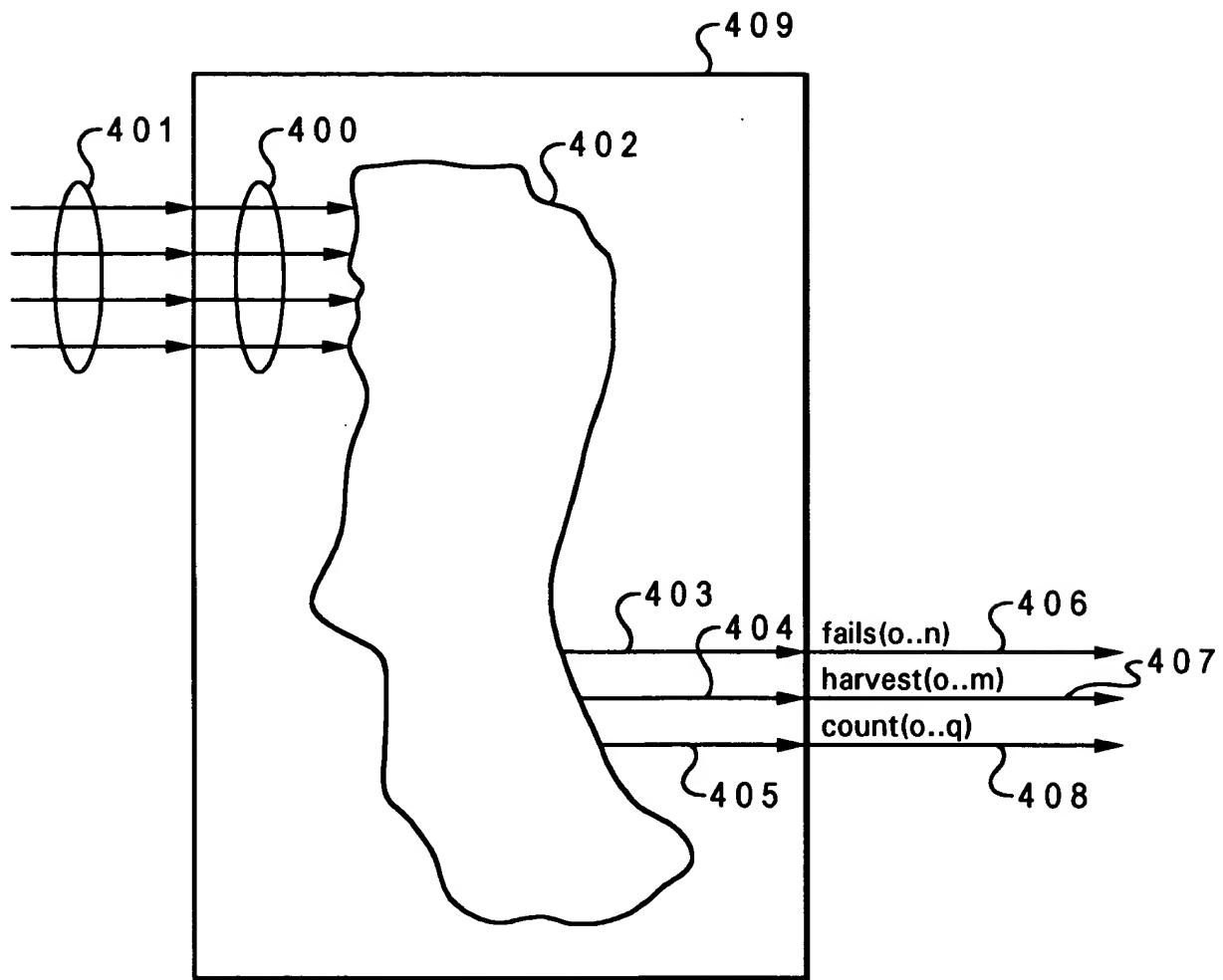


Fig. 4A

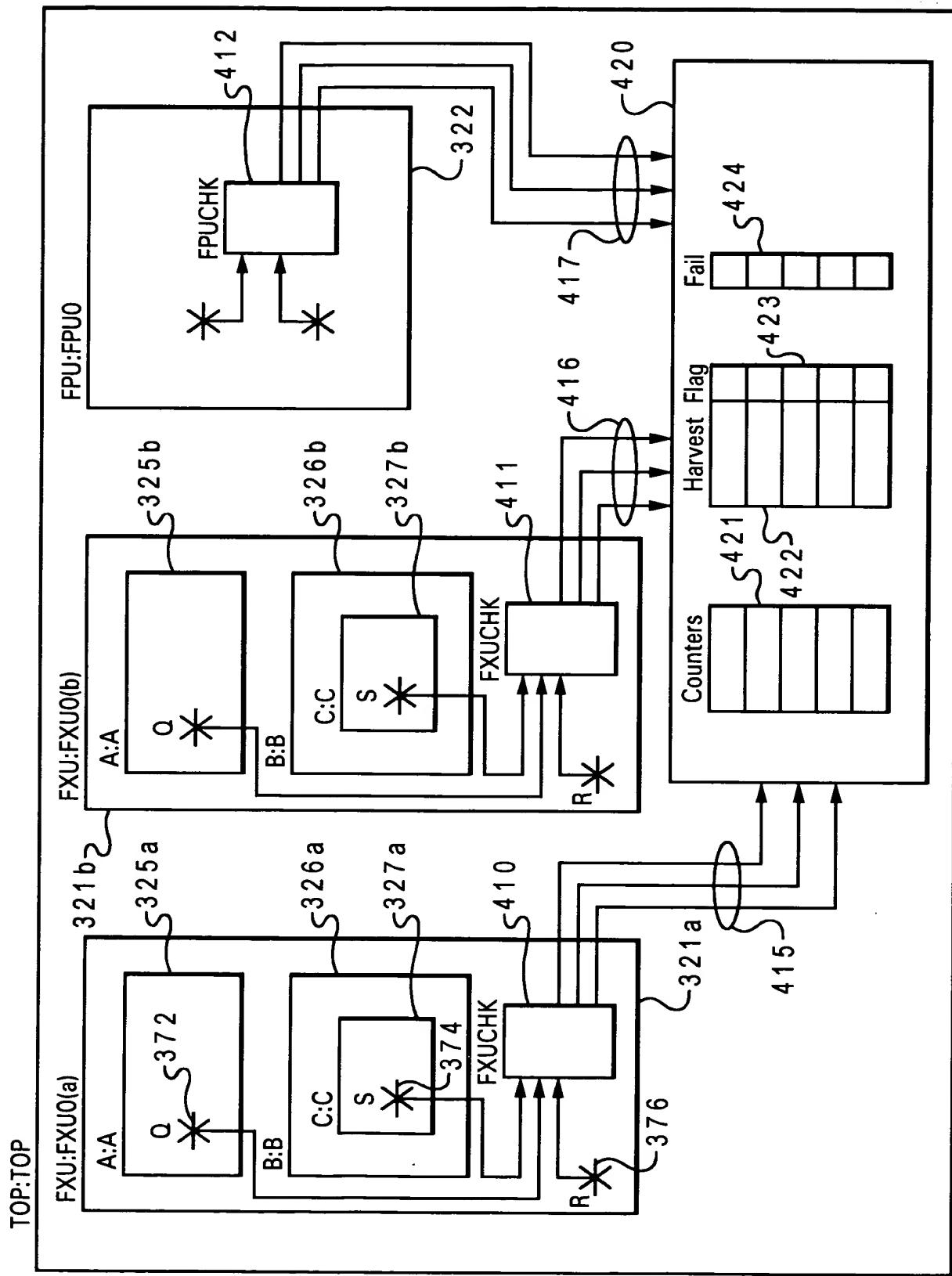


Fig. 4B

329

ENTITY FXUCHK IS

```

PORT( S_IN      : IN std_ulogic;
       Q_IN      : IN std_ulogic;
       R_IN      : IN std_ulogic;
       clock     : IN std_ulogic;
       fails     : OUT std_ulogic_vector(0 to 1);
       counts    : OUT std_ulogic_vector(0 to 2);
       harvests  : OUT std_ulogic_vector(0 to 1));

```

} ;

450 } }

452 { --!! BEGIN  
--!! Design Entity: FXU;

453 { --!! Inputs  
--!! S\_IN => B.C.S;  
--!! Q\_IN => A.Q;  
--!! R\_IN => R;  
--!! CLOCK => clock;  
--!! End Inputs

454 { --!! Fail Outputs;  
--!! 0 : "Fail message for failure event 0";  
--!! 1 : "Fail message for failure event 1";  
--!! End Fail Outputs;

455 { --!! Count Outputs;  
--!! 0 : <event0> clock;  
--!! 1 : <event1> clock;  
--!! 2 : <event2> clock;  
--!! End Count Outputs;

456 { --!! Harvest Outputs;  
--!! 0 : "Message for harvest event 0";  
--!! 1 : "Message for harvest event 1";  
--!! End Harvest Outputs;

457 { --!! End;

440 } }

451 } }

ARCHITECTURE example of FXUCHK IS

```

BEGIN
  ... HDL code for entity body section ...
END;

```

458 } }

Fig. 4C

TOP SECRET//COMINT

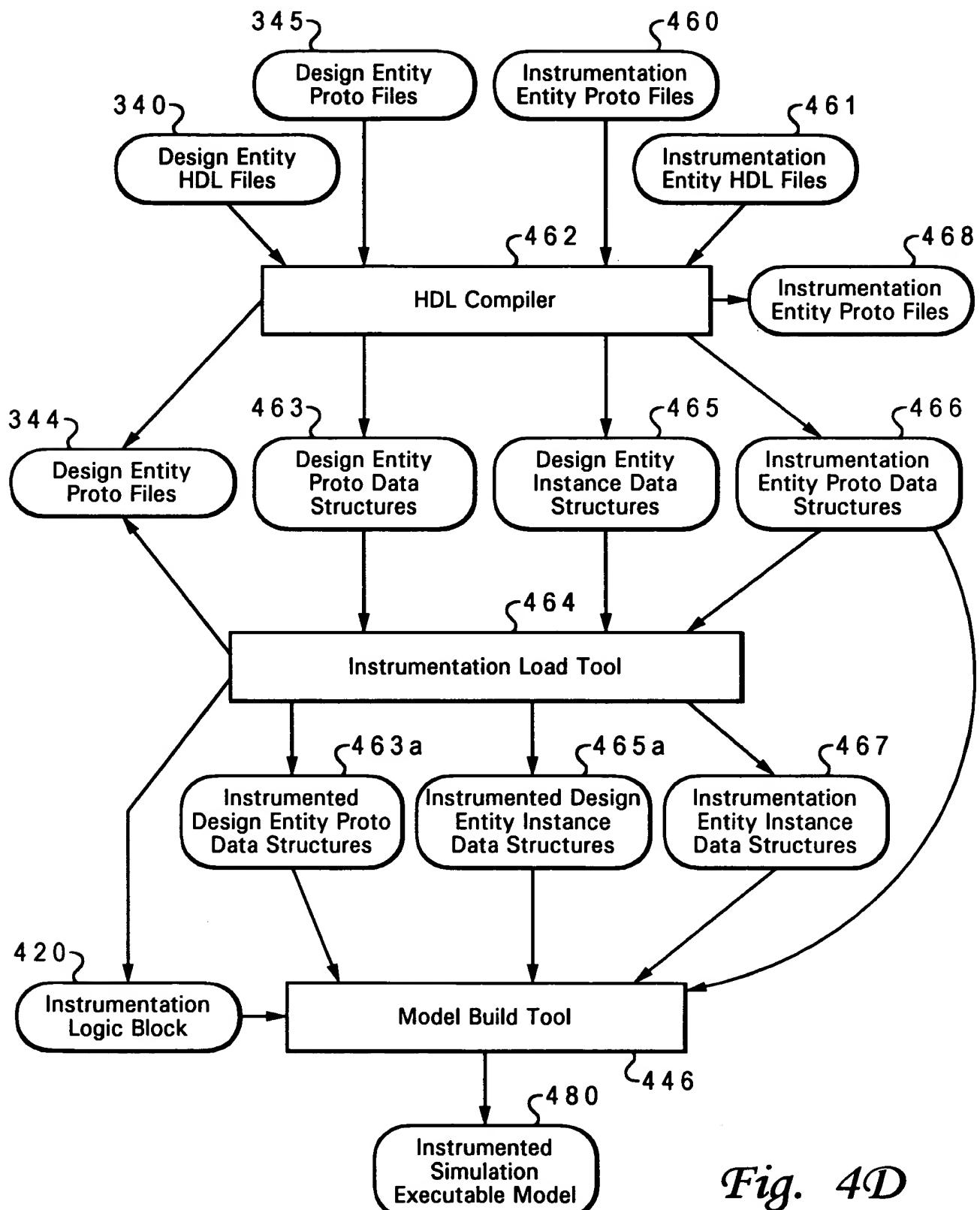


Fig. 4D

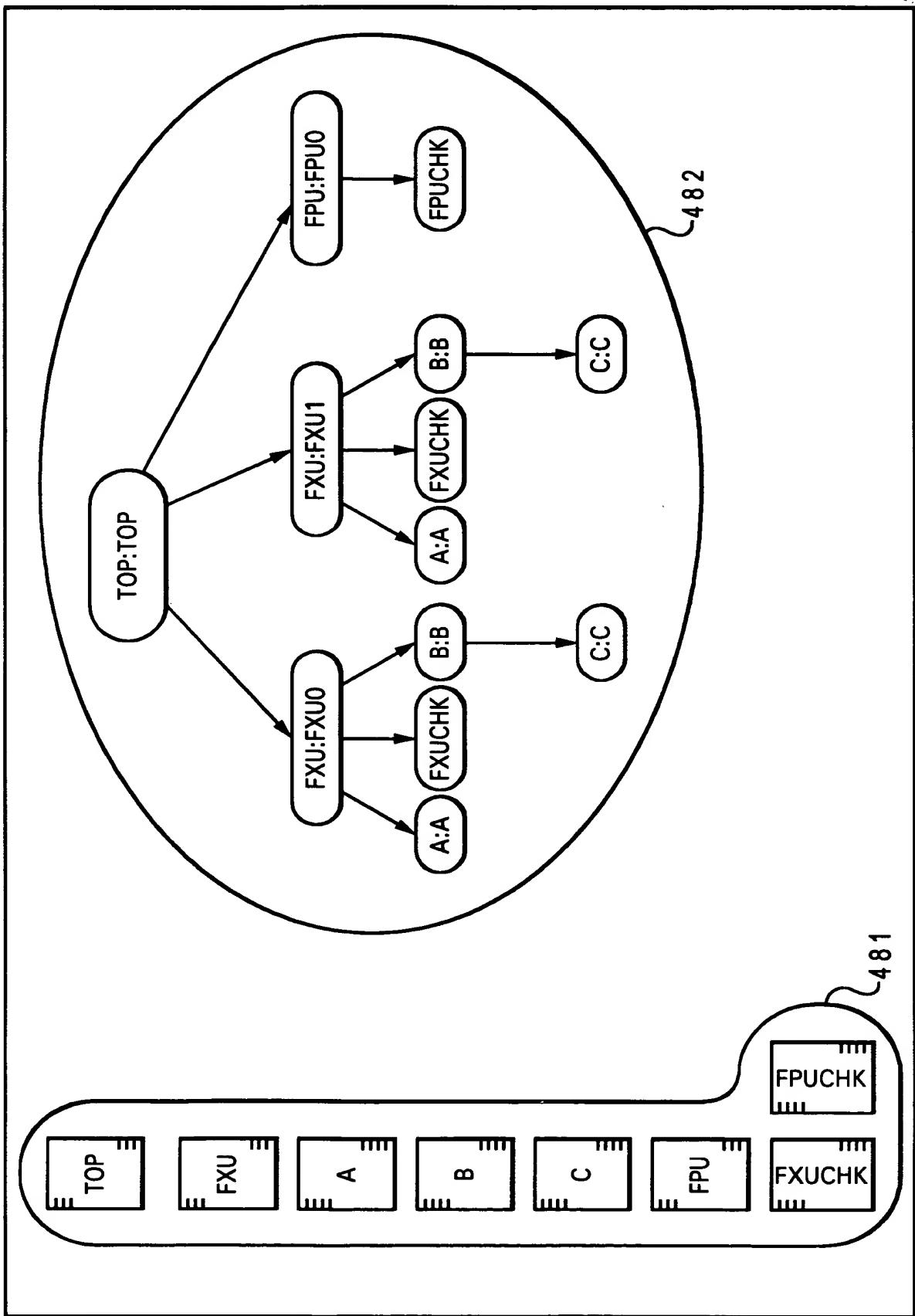


Fig. 4E

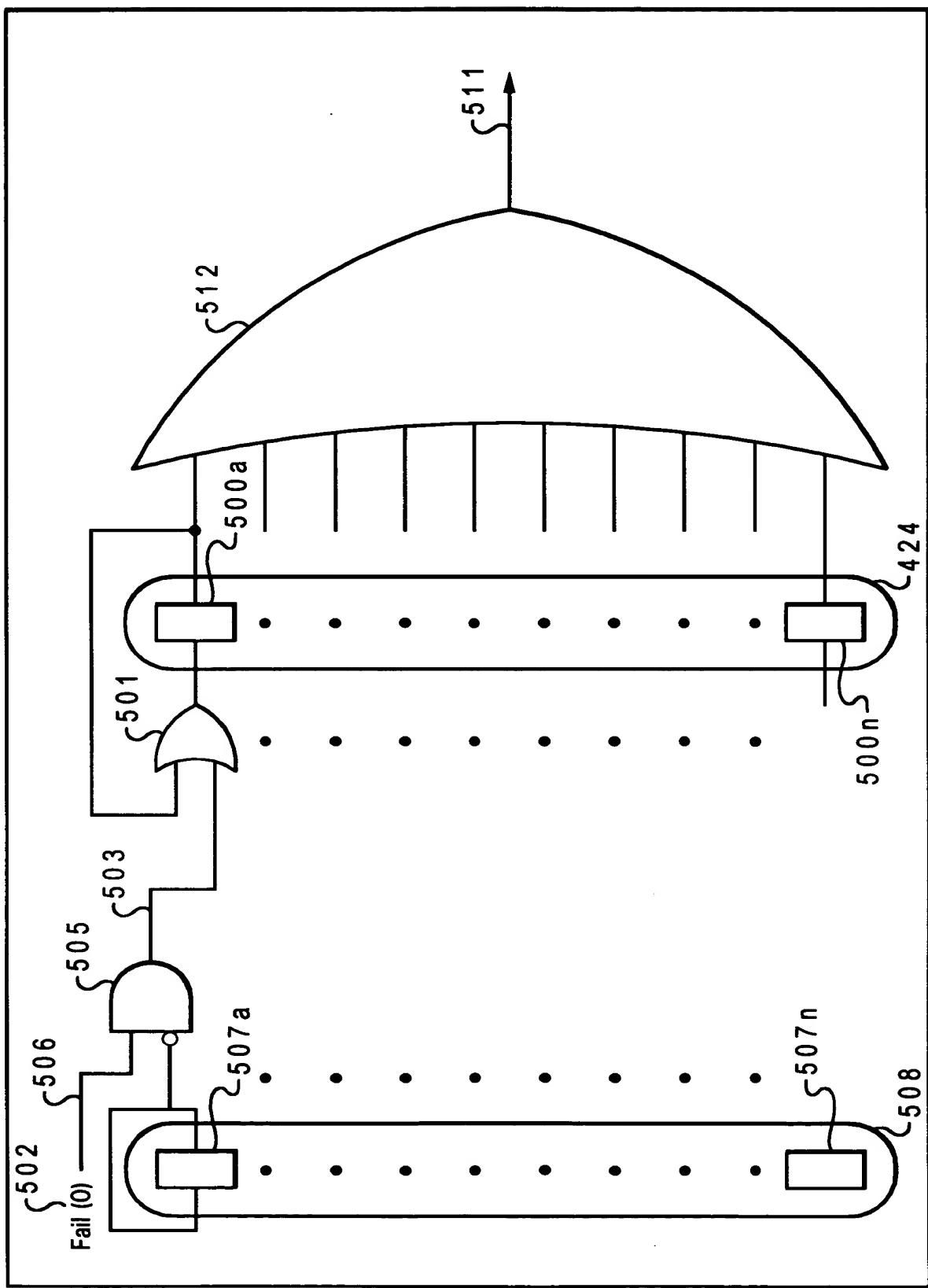
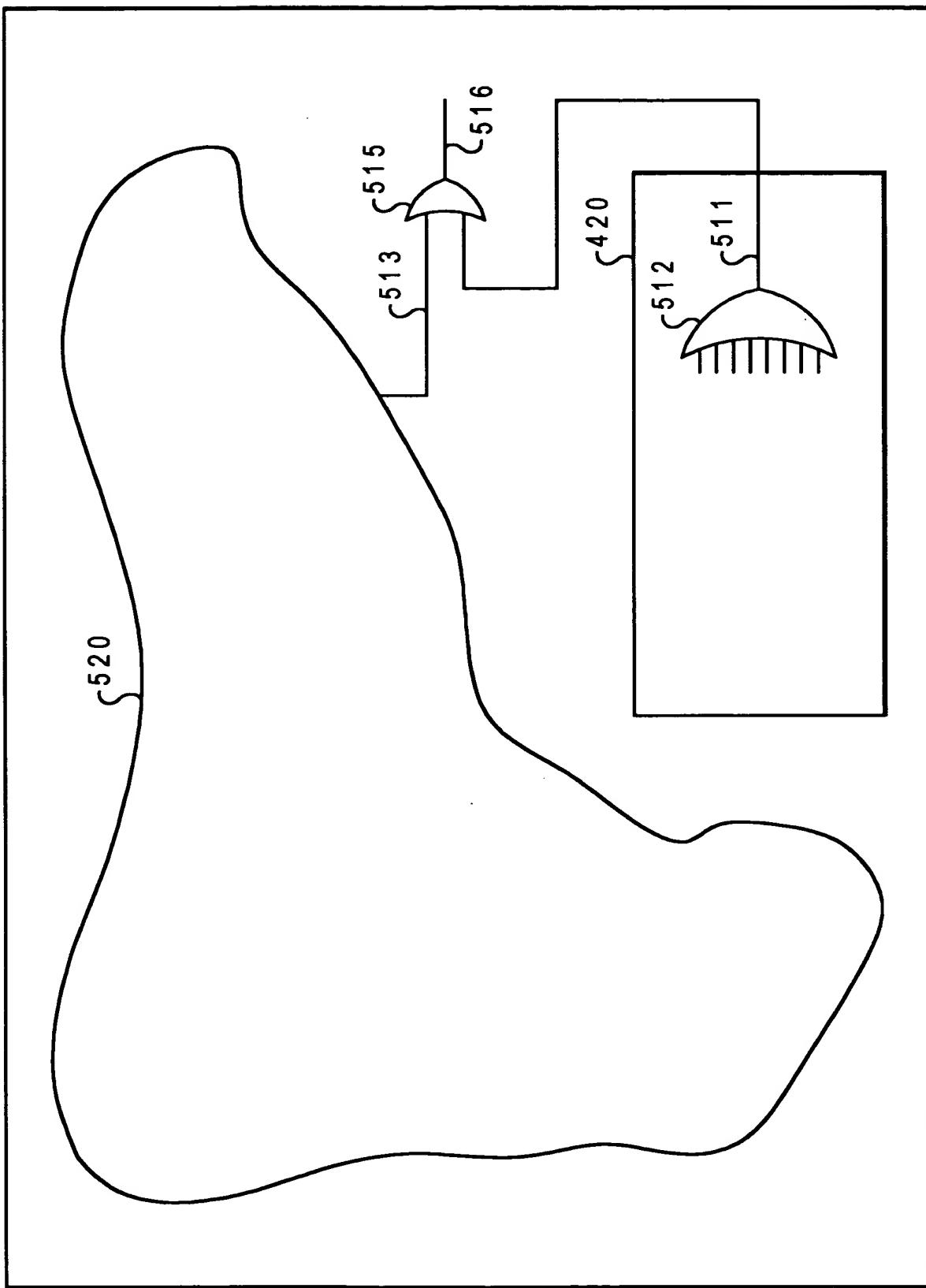
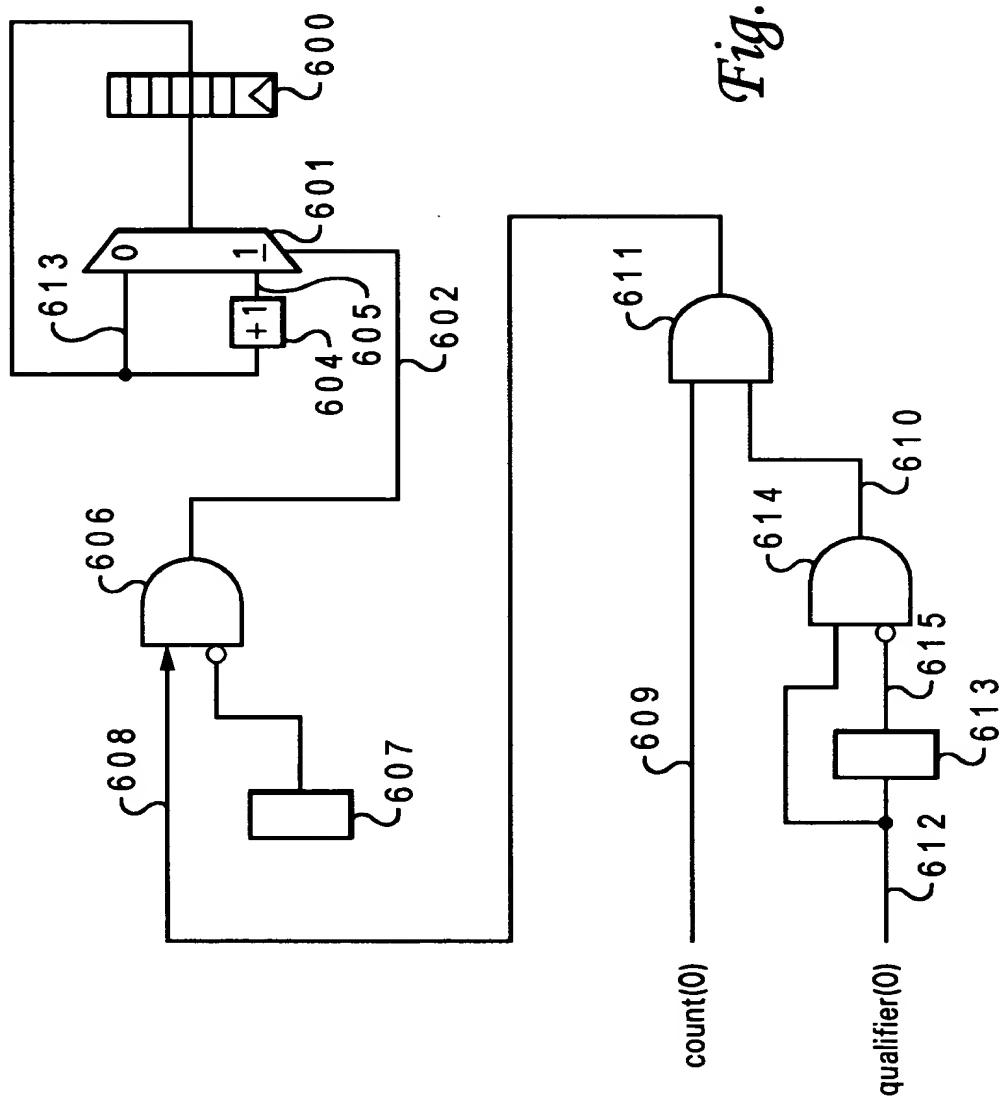


Fig. 5A



*Fig. 5B*

Fig. 6A



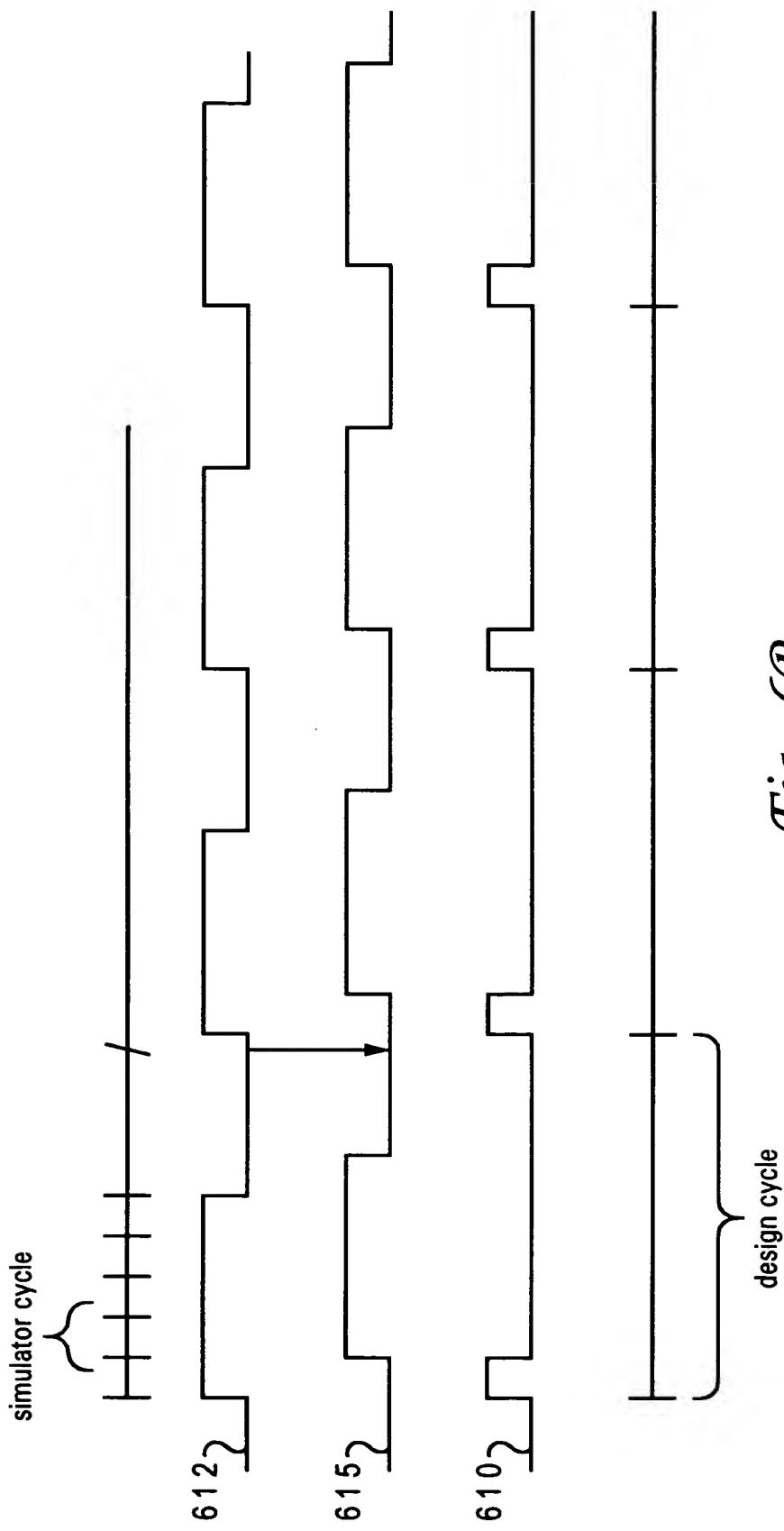


Fig. 6B

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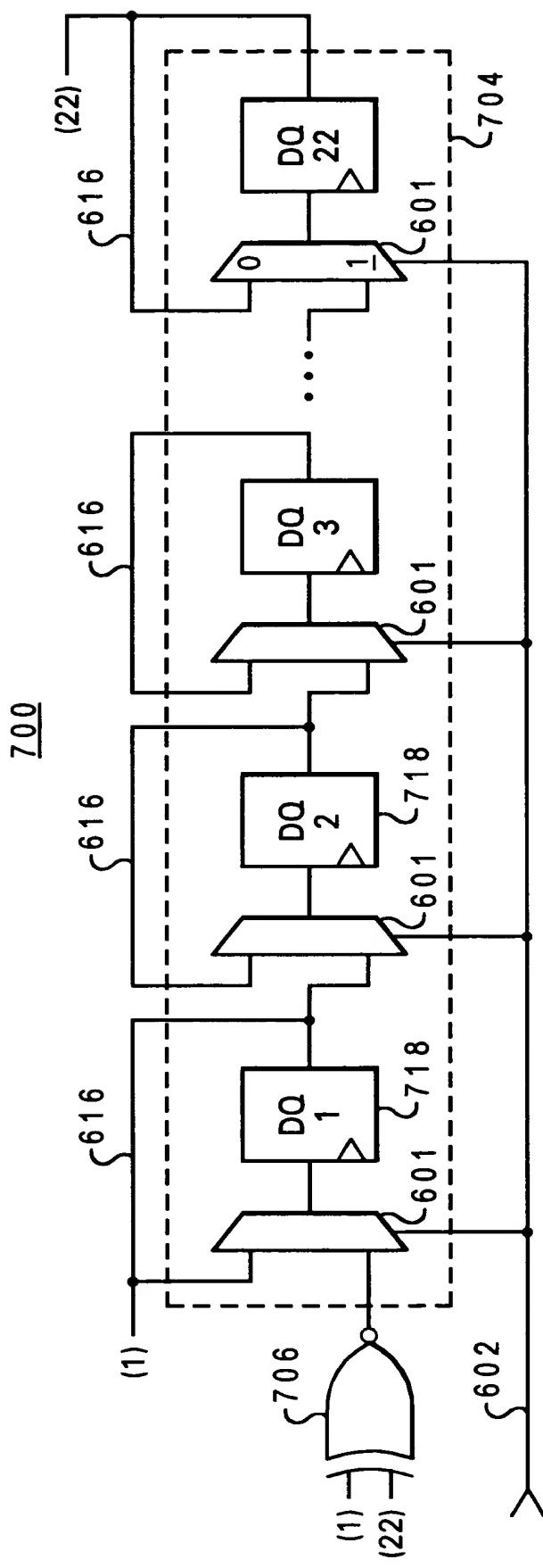
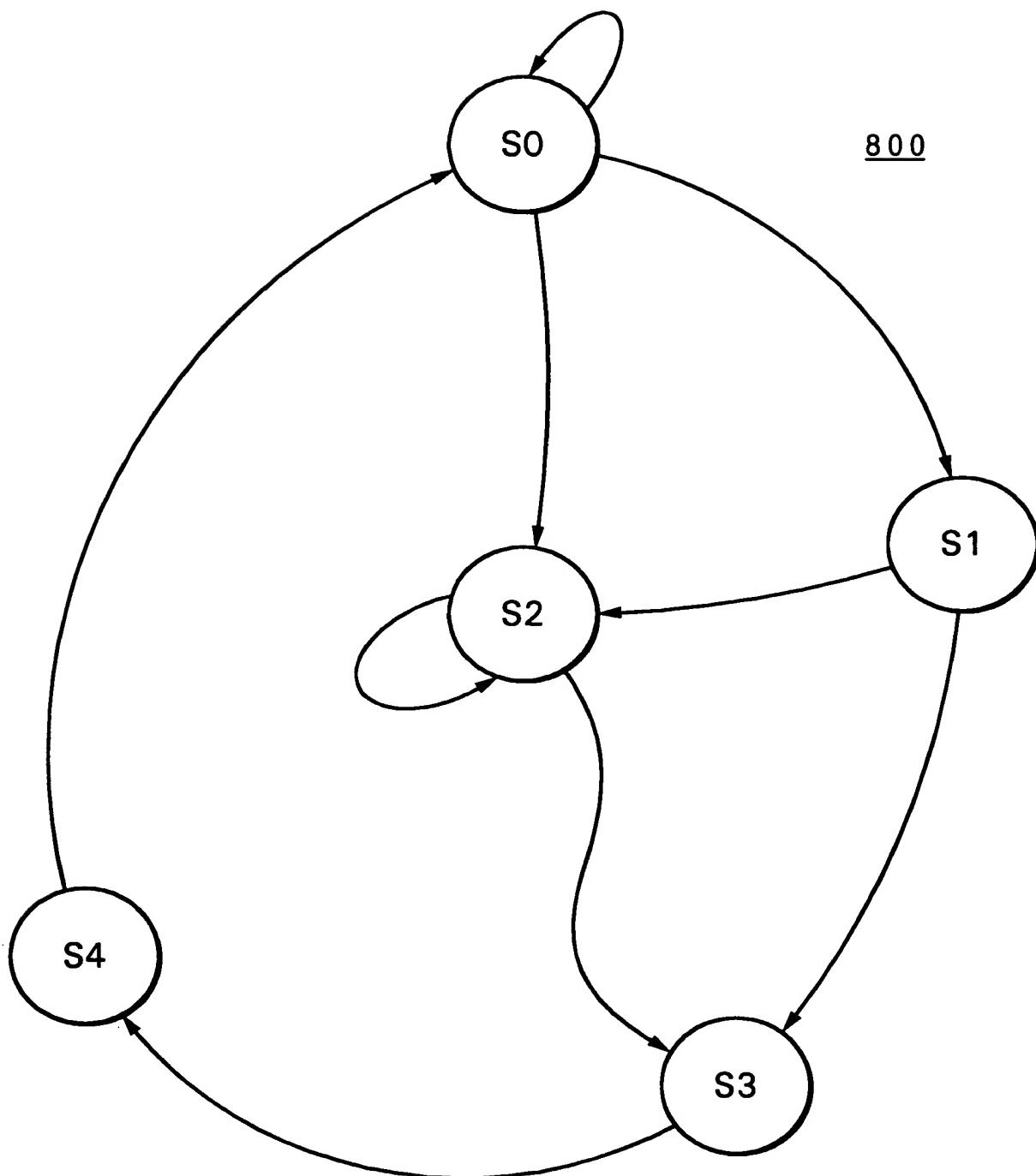


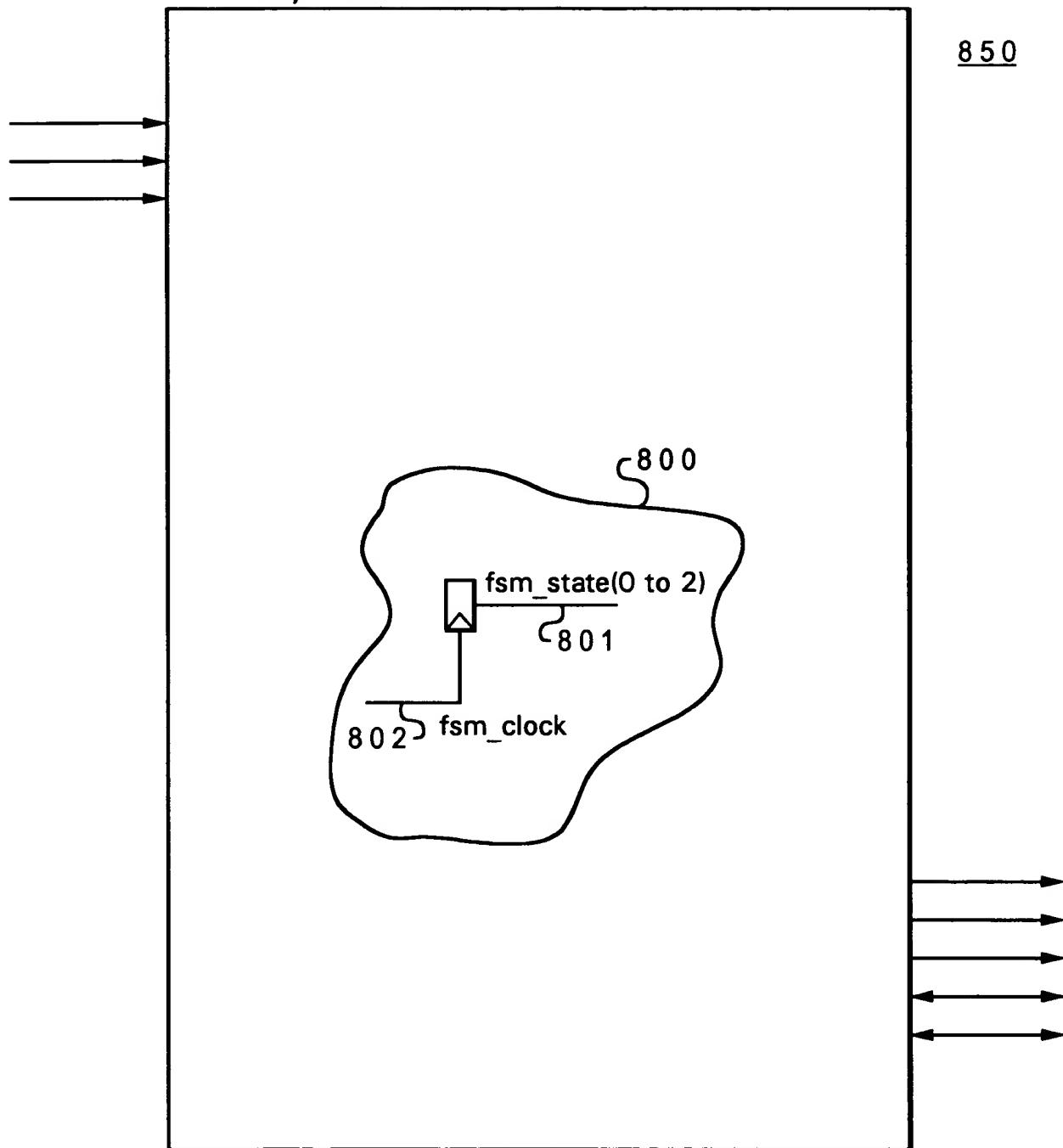
Fig. 7

800

*Fig. 8A  
Prior Art*



entity FSM : FSM

850

*Fig. 8B  
Prior Art*

ENTITY FSM IS

```
PORT(
    ....ports for entity fsm....
);
```

ARCHITECTURE FSM OF FSM IS

BEGIN

... HDL code for FSM and rest of the entity ...

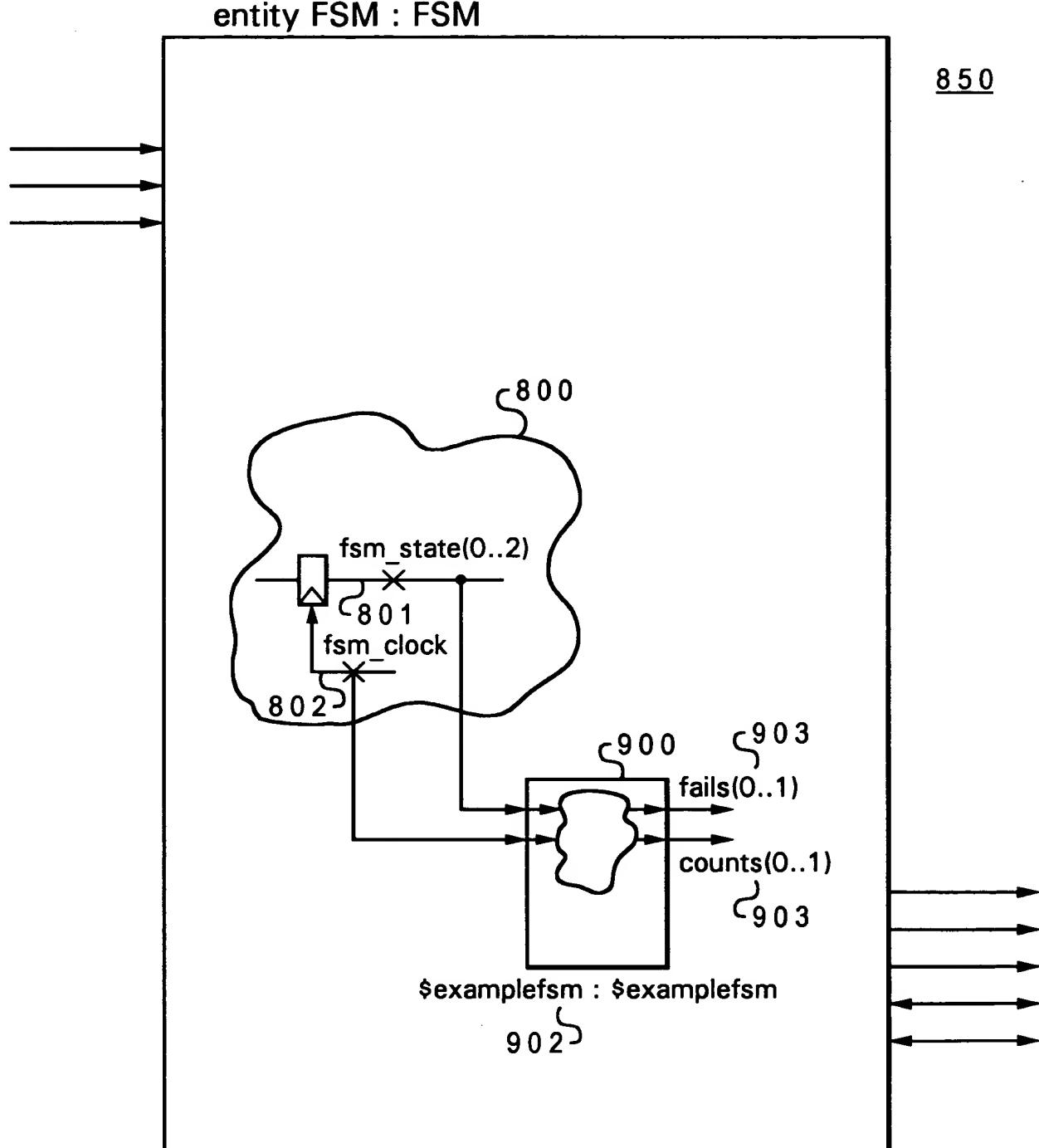
fsm\_state(0 to 2) <= ... Signal 801 ...

```
853 { --!! Embedded FSM : examplefsm;
859 { --!! clock      : (fsm_clock);
854 { --!! state_vector : (fsm_state(0 to 2));
855 { --!! states       : (S0, S1, S2, S3, S4);
856 { --!! state_encoding : ('000', '001', '010', '011', '100');
857 { --!! arcs          : (S0 => S0, S0 => S1, S0 => S2,
     --!!                      (S1 => S2, S1 => S3, S2 => S2,
     --!!                      (S2 => S3, S3 => S4, S4 => S0);
858 { --!! End FSM;
```

852 } 860 }

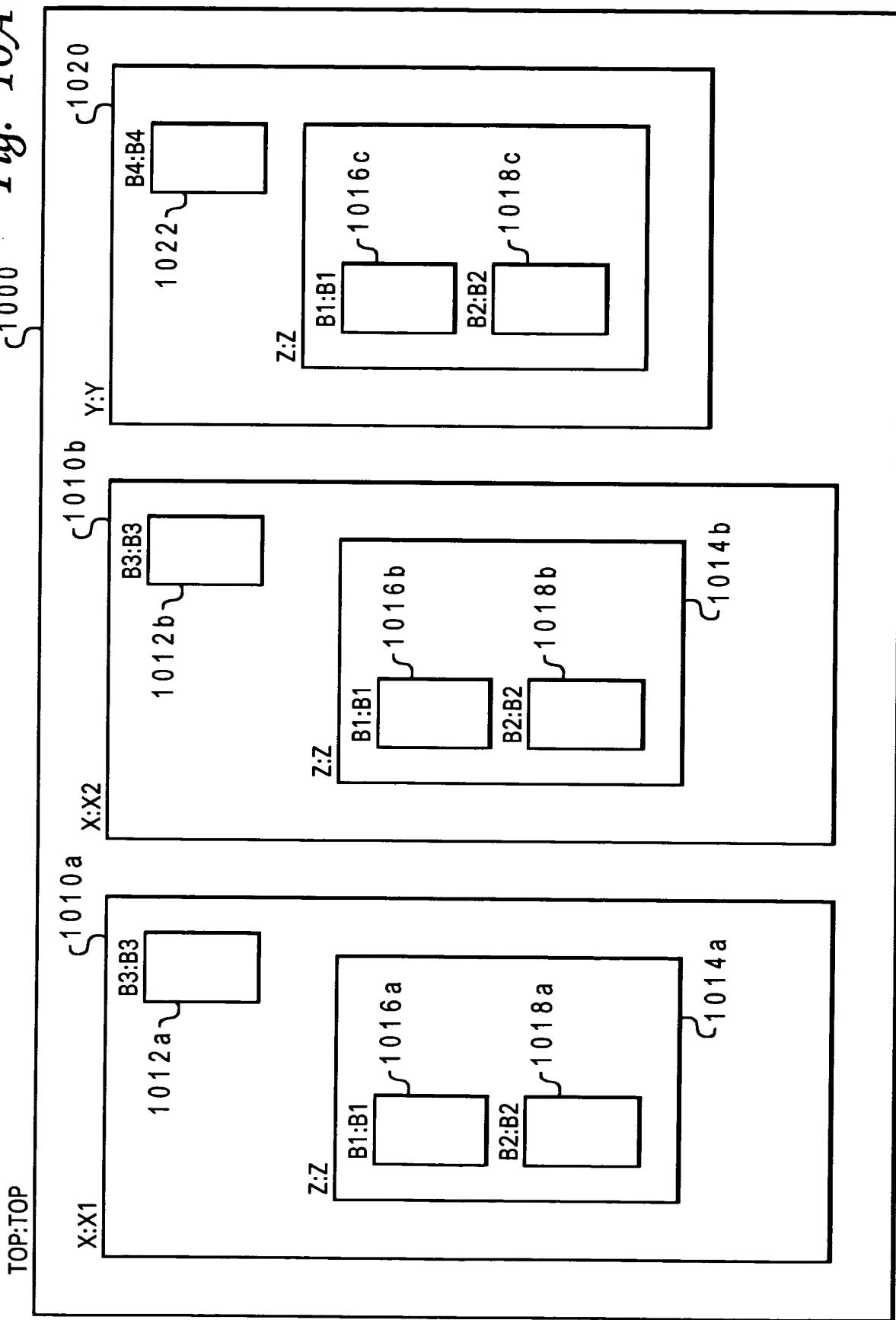
END;

*Fig. 8C*

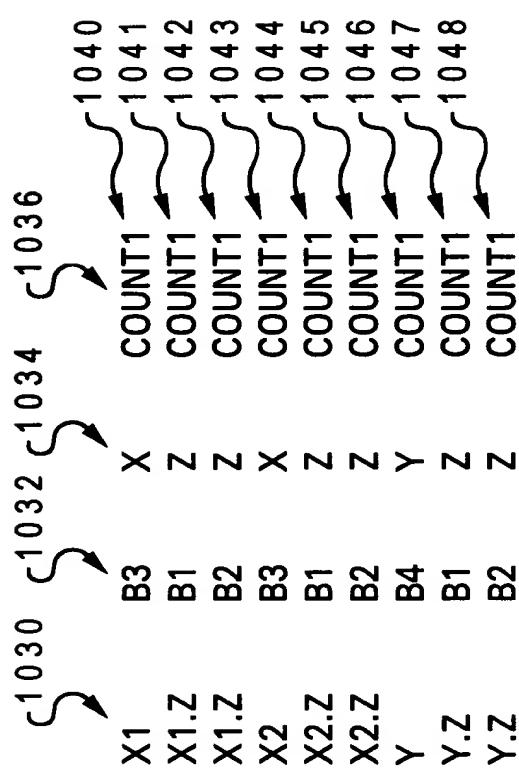


*Fig. 9*

Fig. 10A

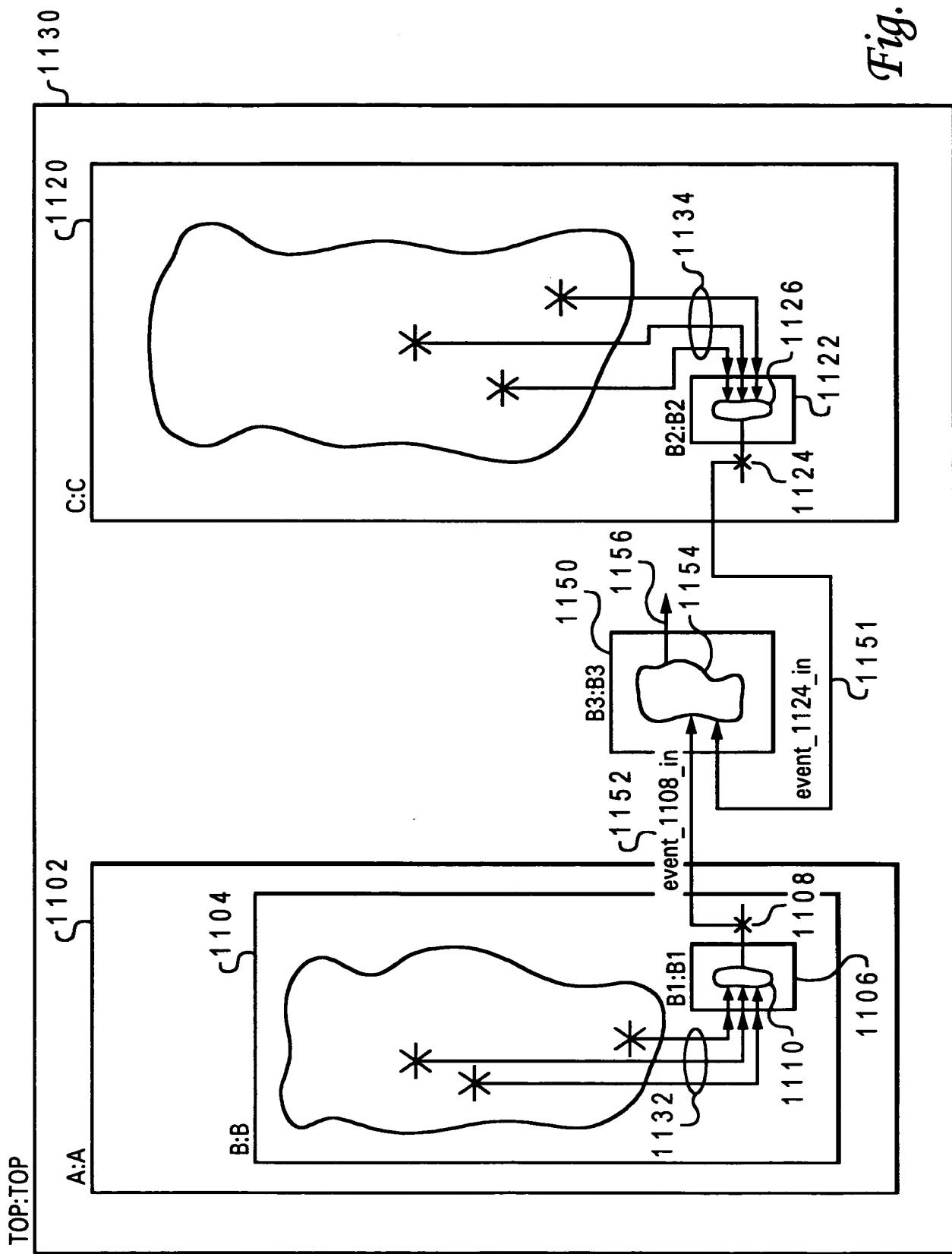


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*Fig. 10B**Fig. 10C**Fig. 10D*

11A

Fig.



--!! Inputs  
--!! event\_1108\_in <= C.[B2.count.event\_1108]; ~~~~~ 1161  
--!! event\_1124\_in <= A.B.[B1.count.event\_1124]; ~~~~~ 1162  
--!! End Inputs

1163                    1165  
1164                    1166  
1161  
1162

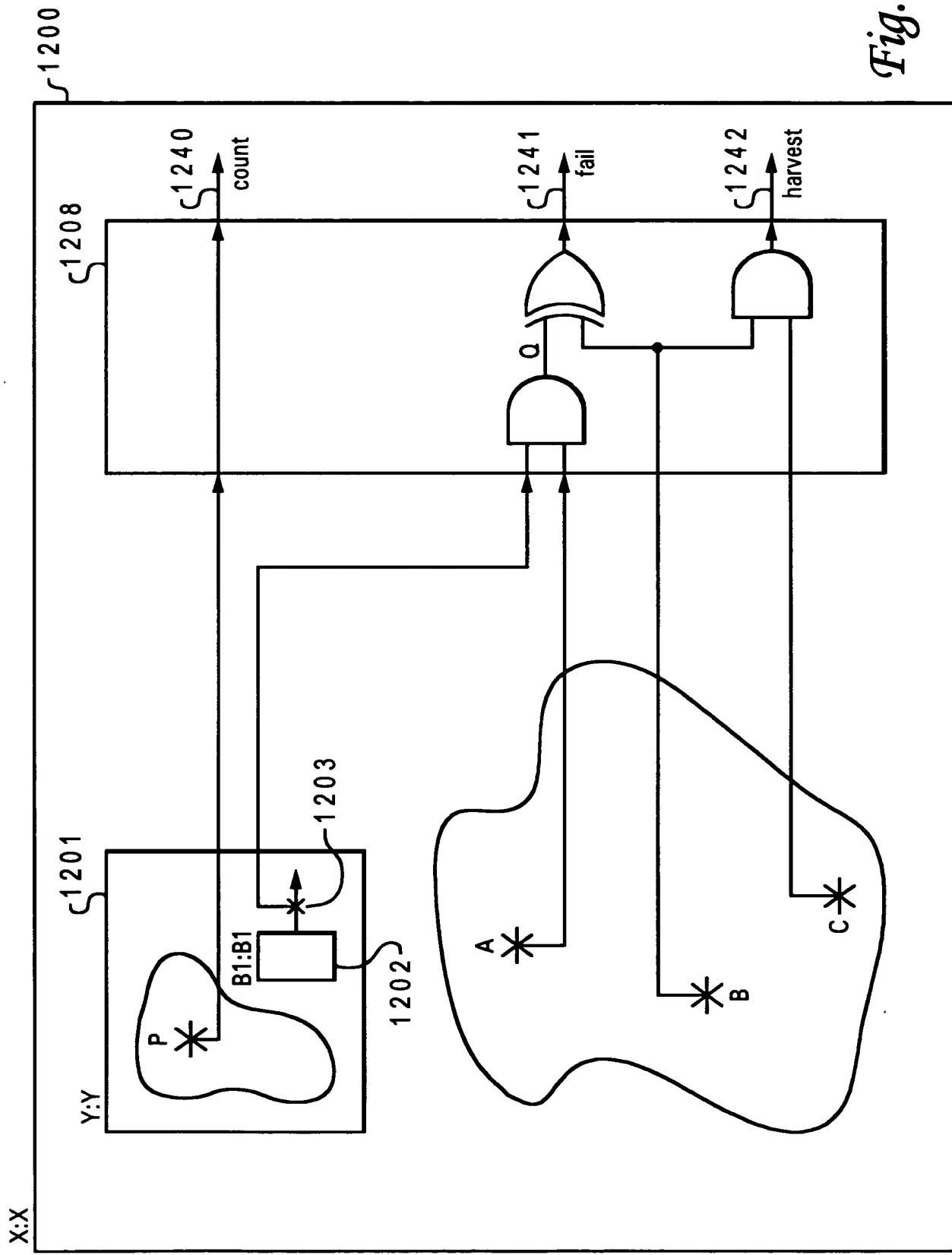
*Fig. 11B*

--!! Inputs  
--!! event\_1108\_in <= C.[count.event\_1108]; ~~~~~ 1171  
--!! event\_1124\_in <= B.[count.event\_1124]; ~~~~~ 1172  
--!! End Inputs

*Fig. 11C*

12A  
AM510912

Fig. 12





ENTITY X IS  
PORT( :  
;  
);

ARCHITECTURE example of X IS  
BEGIN  
. . .  
. . .  
... HDL code for X ...  
. . .  
. . .  
. . .

1220

1221 { Y:Y  
PORT MAP( :  
);

1222 { A <= ....  
B <= ....  
C <= ....

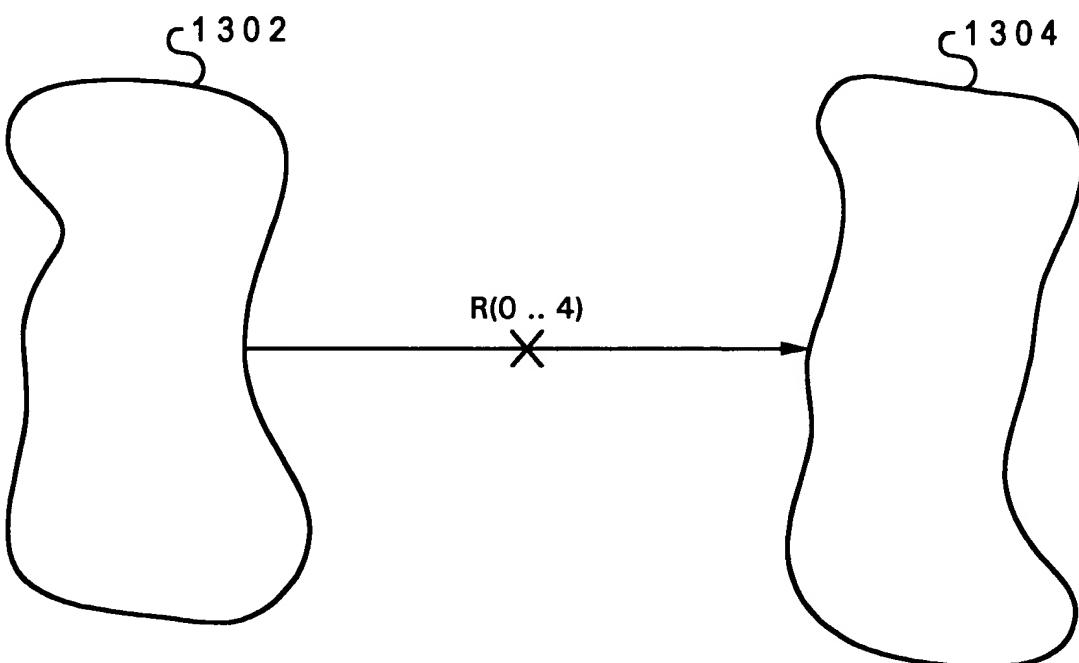
1223 { --!! [count, countname0, clock] <= Y.P; 1230  
--!! Q <= Y. [B1.count.count1] AND A; 1232  
--!! [fail, failname0, "fail msg"] <= Q XOR B; 1234  
--!! [harvest, harvestname0, "harvest msg"] <= B AND C;  
END; 1236

Fig. 12B

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1300



*Fig. 13A*

PCT/EP2010/052460  
SEARCHED  
INDEXED  
TRANSLATED  
FILED  
1300

FOO:FOO

1300

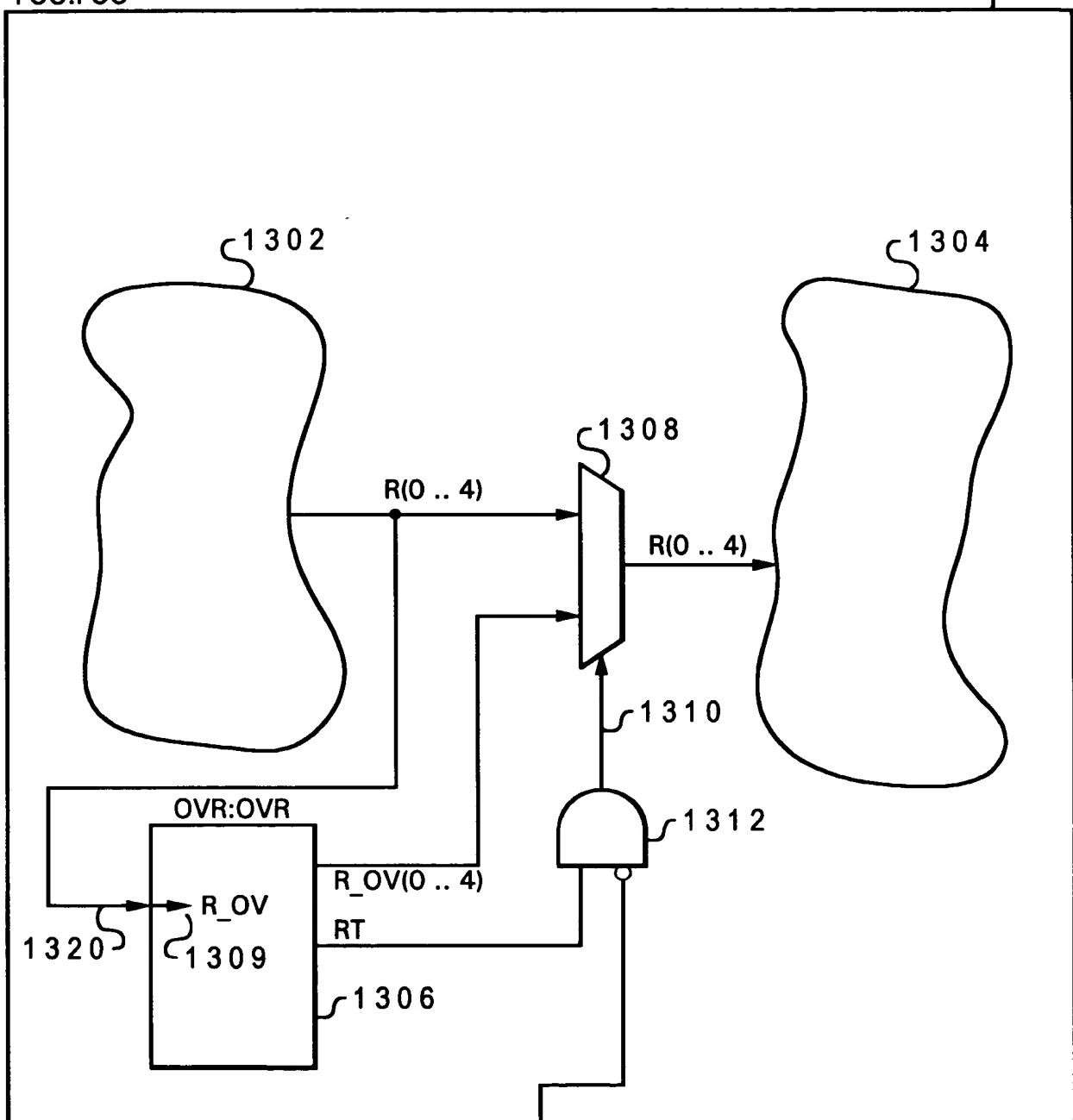
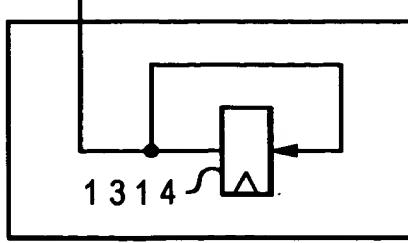


Fig. 13B

1314

420



*Fig. 13C*

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## ENTITY FOO IS

PORT(  
);

## ARCHITECTURE example of FOO IS

BEGIN

$$R \leq \dots$$

1380 {  
 --!! R\_IN <= {R};  
 --!!  
 --!!  
 --!! R\_OV(0 to 4) <= .....; 1383  
 --!! RT <= .....;  
 --!! [override, R\_OVERRIDE, R(0 .. 4), RT] <= R\_OV(0 to 4);  
 } 1384

*Fig. 13D*